Abstract of the Disclosure

The I/O compression test circuit performs the test on the global I/O lines divided into groups when failure occurs, thereby improving the repair efficiency. Also, since the configuration of the test circuit is simplified by using a reset circuit, the delay time generated by a logic circuit device is reduced, thereby decreasing test time. Additionally, two sampling clock signals enable memory cells to perform a stable operation on skew between global I/O lines or glitch generated in internal circuits.